METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION IN A MEMORY ARRAY WITH DYNAMIC WORD LINE DRIVER/DECODERS

ABSTRACT

A memory array includes a storage unit with a number of sections and decoders coupled to respective ones of the sections for decoding an N-bit address signal and responsively asserting a signal on one of the word lines selected by the address signal. Local clock buffers are coupled to respective ones of the decoders for receiving a clock signal and an address signal including M most-significant bits of the N-bit address signal and generating respective timing signals. The decoders receive the timing signal from their respective local clock buffers. Each decoder is operable to alternately precharge and evaluate the N-bit address signal responsive to phases of the timing signal. Each local clock buffer is operable, responsive to a state of the M bits of the address signal, for selecting between holding its timing signal in a deasserted state and enabling its timing signal to follow the clock signal.